



TESSERA 3.3-018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
KHANDROS et al.

Group Art Unit: 2503

Serial No. 08/030,194

Examiner: S. Clark

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For: SEMICONDUCTOR CHIP ASSEMBLIES,
METHODS OF MAKING SAME AND
COMPONENTS FOR SAME

X
Assistant Commissioner For Patents
Washington, D.C. 20231

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Sir:

INFORMATION DISCLOSURE STATEMENT

GROUP 2500

It is respectfully requested that the references listed on the enclosed Form PTO-1449 be made of record and considered with respect to the above-referenced U.S. Patent application. A copy of each reference is enclosed, except that copies of references which were of record in the parent applications are not enclosed. One Japanese-language reference is enclosed; a translation is provided herewith. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material. Comments concerning the relevance of certain references are included in the accompanying amendment and response.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231 on June 26, 1995.

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